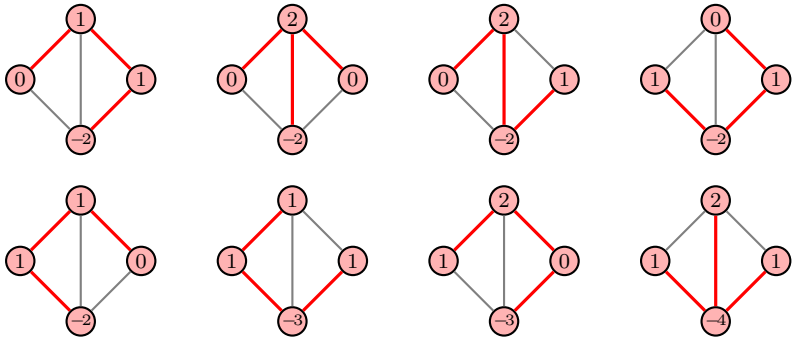
Topics: Chip firing

1. Let $G = K_4 \setminus \{1, 3\}$. The eight critical chip configurations are shown below, along with the result of Dhar's burning test, and the corresponding spanning tree.



Recall that the critical configurations form a group called the *critical group*, denoted $\mathcal{K}(G)$, where the operation is defined as

$$[\boldsymbol{c}_1] + [\boldsymbol{c}_2] = [\boldsymbol{c}_1 + \boldsymbol{c}_2].$$

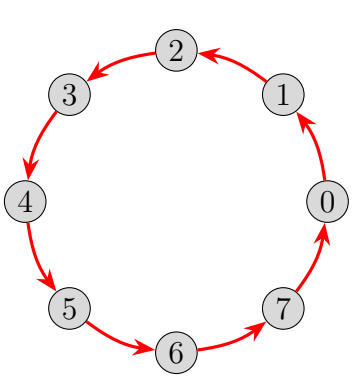
(a) The reduced Laplacian is $L_0(G) = \begin{bmatrix} 2 & -1 & 0 \\ -1 & 3 & -1 \\ 0 & -1 & 2 \end{bmatrix}$, and its determinant is $d_3 = 8$. Compute the greatest common divisor of all 2×2 minors; call this d_2. Then compute d_1, the GCD of all 1×1 minors. The sequence $d_1 \mid d_2 \mid d_3$ are the *elementary divisors* of the so-called *Smith normal form*, and they determine the critical group.

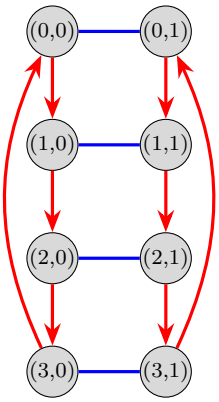
(b) What is the identity element of $\mathcal{K}(G)$? That is, what chip configuration $\boldsymbol{c}_0$ satisfies $[\boldsymbol{c}_0] + [\boldsymbol{c}] = [\boldsymbol{c}]$ for every $[\boldsymbol{c}] \in \mathcal{K}(G)$?

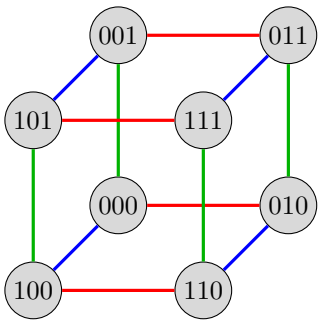
(c) Which (non-identity) chip configurations are their own inverses? That is, which satisfy $[\boldsymbol{c}] + [\boldsymbol{c}] = [\boldsymbol{c}]$? Use this to determine whether $\mathcal{K}(G)$ is isomorphic to $\mathbb{Z}_8$, $\mathbb{Z}_4 \times \mathbb{Z}_2$, or $\mathbb{Z}_2 \times \mathbb{Z}_2 \times \mathbb{Z}_2$.

(d) Construct an 8×8 *Cayley table* for $\mathcal{K}(G)$.

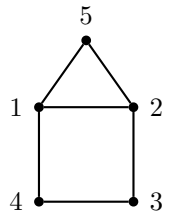
(e) Construct a *Cayley graph* of $\mathcal{K}(G)$, and put the chip configurations in the corresponding nodes. It will have the form of one of the following







2. Consider the "house graph" G shown below:



(a) Find the Laplacian $L(G)$ and compute $\det(L_0(G))$.

(b) Construct all critical chip configurations. Which is the identity element of $\mathcal{K}(G)$?

(c) Run Dhar's burning test on the critical configurations and associate each with a spanning tree.

(d) Construct all superstable chip configurations.

(e) Construct a Cayley graph with the nodes labeled by the corresponding chip configurations.